Zero-voltage transition bridgeless single-ended primary inductance converter power factor correction rectifier

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Abstract: In this study, a new zero-voltage transition (ZVT) bridgeless single-ended primary inductance converter power factor correction converter is introduced. The proposed converter has only two semiconductor elements in the current path at any time. Therefore the conduction losses in this converter are reduced in comparison with conventional SEPIC PFC rectifier. Also, in the proposed converter, ZVT soft switching technique is applied to improve the efficiency. The principle of the operation, design procedure and simulation results are presented. A 450 W prototype of this converter is implemented and the experimental results are presented to demonstrate the feasibility of the proposed technique.

1 Introduction

Nowadays, dc power voltage supplies are widely used in electronic equipment. Therefore employing ac/dc converters such as the conventional diode bridge is unavoidable, which results in low-power factors of about 0.5–0.7 [1]. Owing to the problems created by these non-linear loads, standards such as IEC61000-3-2 are established to limit the current and thus it is a good candidate for PFC. Active PFC converters are very attractive because of their low-input harmonics for various load conditions. A conventional active PFC is a bridge rectifier followed by a dc/dc converter. Boost converter is widely used as the dc/dc converter in PFC because of its low cost, high performance and simplicity [3]. Boost-type PFC converter suffers from many drawbacks that include: (1) the dc output voltage is always higher than the peak input voltage, (2) input–output isolation cannot be implemented easily, (3) the startup inrush current is high and (4) there is a lack of current limiting during overload conditions [4]. In [5] a comparative study between some basic PFC topologies is presented. To overcome the problems associated with the boost-type PFC converters, especially in universal input voltage applications where the output voltage is lower than the input voltage (e.g. in telecommunication applications or computer industry), the step up/down converters are required [6–8].

To increase the efficiency of boost PFC converter, a new method called bridgeless PFC converter or dual boost PFC converter is reported [9]. Fig. 1 shows the conventional PFC converter and regular bridgeless boost PFC. In this method, two boost PFC converters are used for each half-line cycles. As a result, the conduction losses are reduced by 1/3 with respect to conventional PFC converter [9]. Other converters such as single-ended primary inductance converter (SEPIC), Cuk, buck–boost and buck converters are used in bridgeless configuration [8, 10–19] to overcome the problems associated with boost PFC. In the bridgeless buck PFC converters presented in [10, 11], the input current cannot follow the input voltage at zero crossings of the input voltage. This is because of the fact that the buck converter cannot perform properly as a PFC whenever the output voltage is higher than the input voltage. In [12, 13] there are three semiconductor elements in the power flow path of the bridgeless buck–boost PFC converter. Therefore the efficiency is not improved in comparison with the conventional counterpart. The buck and buck–boost PFC converters have discontinuous input current. Also, zero-crossing problem of input current is very severe when buck converter is used. Unlike the Cuk converter, SEPIC does not have negative output voltage and also does not suffer from the above mentioned problems and thus it is a good candidate for PFC.

Fig. 2 shows the conventional SEPIC PFC converter. Bridgeless PFC rectifiers based on the SEPIC topology are presented in [8, 14–18]. In [19], an attractive topology is proposed as a bridgeless SEPIC PFC converter. The number of elements used in this converter is reduced in comparison with other proposed SEPIC PFC converters [8, 14–18] and also the gate driver of this converter is connected to ground.

Recently, various soft switching techniques are applied to bridgeless boost PFC converters to further improve the efficiency by reducing the switching losses [20–25].
(ZCT) are soft switching techniques that provide soft switching while the desirable features of conventional pulse-width modulation (PWM) converters remain. ZVT techniques eliminate the turn on capacitive losses and thus metal-oxide semiconductor field-effect transistors are preferred. However, at high-power applications, insulated gate bipolar transistors (IGBTs) are used because of their lower conduction losses and cost. To eliminate tailing current problem of IGBTs, ZCT techniques are preferred. The presented topology in [26] is a combination of bridgeless SEPIC rectifier and a ZVT technique. Therefore in the present paper, a soft switching technique is applied to a bridgeless step up/down (SEPIC) converter to further increase the efficiency.

In the next section of this paper, the operation of the proposed converter is analysed. In Section 3, the converter design procedure is presented. To show the validity of the theoretical analysis, the converter is designed in Section 4 and computer simulation results are provided. The experimental results from the implemented prototype are
presented in Section 5. Finally, the drawn conclusions are presented in Section 6.

2 Proposed bridgeless PFC circuit operation

Fig. 3a shows the power stage of the proposed soft switching bridgeless SEPIC PFC rectifier. In this circuit, the SEPIC converter is combined with the input rectifier to reduce the conduction losses. In this converter, an auxiliary circuit (as shown in the dotted box) is used to provide zero-voltage switching (ZVS) condition. Soft switching at turn off instant is provided by Cr and other elements provide ZVS condition at turn on instant. The operation of this converter is symmetrical in two half-line cycles of input voltage. Therefore the converter operation is explained during one switching period in the positive half-line cycle of the input voltage. The operation of this converter is similar to the conventional bridgeless SEPIC rectifier except at the switching instants. In order to simplify the analysis, it is assumed that the converter operates in continuous conduction mode (CCM). Also, it is supposed that the converter is operating at steady-state condition and all circuit elements are ideal. In addition, the output capacitance is assumed sufficiently large to be considered as an ideal dc voltage source ($V_O$). Also, the input voltage is assumed constant and equal to $V_{ac}(t_0)$ during a switching cycle. Similarly, the input voltage, input current and $L_3$ current are assumed constant in a switching cycle. Based on the above assumptions, the equivalent circuit in the positive half-line cycle is shown in Fig. 3b. The elements used in the negative half-line cycle are shown by grey colour.

The circuit operation in a switching cycle can be divided into six modes as shown by the equivalent circuits in Fig. 4. In this figure, the bolded lines show the current flow path. The theoretical waveforms are illustrated in Fig. 5. Before the first mode, it is assumed that the converter is in power-transferring mode, $i_{L1}=0$ and $V_{C1}=V_O+V_{ac}(t_0)$. Therefore $D_1$ and $D_p$ are conducting and all other semiconductor devices are off. Note that the voltage of $C_1$ follows the input voltage in CCM.

- **Mode 1:** [$t_0$–$t_1$] (Fig. 4a): This mode starts by turning $S_3$ on to provide ZCS condition for the main switch $S_1$. Thus, $L_r$ current increases linearly with slope of $(V_O+V_{ac}(t_0))/L_r$. This mode lasts until the $L_r$ current becomes zero. The main switch can be turned on during this interval. It must be noted that because of the sinusoidal shape of auxiliary switch, this switch turns on and off under ZCS condition in

$$t_1 - t_0 = \frac{(V_O+V_{ac}(t_0))}{L_r(i_{in}+i_{L3})}$$

- **Mode 2:** [$t_1$–$t_2$] (Fig. 4b): When $i_{L1}$ reaches $i_{in}+i_{L3}$ the output diode ($D_3$) is turned off under zero-current condition. Then a resonance between $L_r$ and $C_r1$ begins. Therefore $V_{C1}$ and $i_{L1}$ can be calculated from the following equations. This mode lasts until the $L_r$ current becomes zero. The main switch can be turned on during this interval. It must be noted that because of the sinusoidal shape of auxiliary switch, this switch turns on and off under ZCS condition in

Fig. 4 Equivalent circuit of each operating mode

a Mode 1  d Mode 4
b Mode 2  e Mode 5
c Mode 3  f Mode 6
To provide soft switching condition $i_L$ should become zero therefore (4) must be satisfied

$$i_{Lr}(t) = i_{in} + i_{L3} + \frac{V_O + V_{in}(t_0)}{Z_r} \sin(\omega_r(t - t_1))$$  \hspace{1cm} (2)$$

$$V_{C1}(t) = (V_{in}(t_0) + V_O) \cos(\omega_r(t - t_1))$$  \hspace{1cm} (3)$$

$$Z_r \leq \frac{V_O + V_{in}(t_0)}{i_{in} + i_{L3}}$$  \hspace{1cm} (4)$$

where

$$Z_r = \sqrt{\frac{L_r}{C_r}}$$  \hspace{1cm} \omega_r = \frac{1}{\sqrt{L_r C_r}}$$

Thus, duration of this mode can be calculated by setting $i_{Lr}(t) = 0$.

- **Mode 3:** $[t_2-t_3]$ (Fig. 4c): In this mode, $C_{r1}$ is charged by $i_{in} + i_{L3}$ linearly. This mode is finished when the voltage of $C_r$ reaches zero. Thus, the main switch turns on under ZVS condition. The duration of this mode can be calculated from the following equation

$$t_3 - t_2 = \frac{C_r V_{C1}(t_2)}{i_{in} + I_O}$$  \hspace{1cm} (5)$$

- **Mode 4:** $[t_3-t_4]$ (Fig. 4d): In this mode, the main switch is conducting and the input inductor is being charged. This mode is similar to the on time of the main switch in the conventional hard switching SEPIC converter. This mode lasts until the main switch is turned off by the controller.

- **Mode 5:** $[t_4-t_5]$ (Fig. 4e): By turning off the main switch, this mode starts and the $C_r$ is charged linearly by the $i_{in} + i_{L3}$ current. Thus, the main switch voltage increases linearly to $V_O + V_{in}(t_0)$. Consequently, the main switch is turned off under ZVS condition. The duration of this mode can be calculated from the following equation

$$t_4 - t_3 = \frac{C_r (V_O + V_{in}(t_0))}{i_{in} + I_O}$$  \hspace{1cm} (6)$$

- **Mode 6:** $[t_5-T_s]$ (Fig. 4e): In this mode the output diode (D3) is turned on under ZVS condition and the $I_{in} + I_O$ is transferred to the output. This mode lasts until the end of the switching cycle ($T_s$).

## 3 Design procedure and efficiency improvement

As mentioned in the previous sections, the operation of this converter is like conventional SEPIC PFC converter except at the switching instants. The operation and design procedure for the main converter elements are provided in the [7, 8]. Therefore in this section design guidelines for designing the auxiliary circuit are discussed. Also the procedure to produce the gate signal for the auxiliary switch is explained.

### 3.1 Auxiliary circuit design

The proposed converter operation is like the conventional converter except at the switching instants and thus, the switching transients can be neglected in comparison with the rest of switching time. As a result, the resonant frequency of the auxiliary circuit is selected ten times greater than the switching frequency. Therefore the following relation is established.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = 10f_{sw}$$  \hspace{1cm} (7)$$

Another equation is needed to determine $L_r$ and $C_r$ values. This equation is obtained from soft switching condition. Based on the PFC of the converter, the input current and input voltage are

$$I_{in}(t) = I_1 \sin(\omega t)$$

$$V_{ac}(t) = V_1 \sin(\omega t)$$  \hspace{1cm} (8)$$

Therefore

$$I_1 = \frac{2P_O}{V_1 \eta}$$  \hspace{1cm} (9)$$

where $P_O$ is the output power and $\eta$ is the efficiency of the
The output current \(I_o\) is the average of \(L_3\) current. Thus
\[
i_{L3}(t) = I_o |\sin(\omega t)|
\]
and
\[
I_o = \frac{P_o}{V_o} = \langle i_{L3}(t) \rangle = \frac{2}{\pi} I_o
\]
where \(I_o\) is the maximum of \(L_3\) current.

Based on the circuit operation in the previous section, at all times (4) must be true to provide soft switching condition. By substituting (8), (9) and (11) into (4), at the worst case, the following equation is determined
\[
Z_r \leq \frac{V_o + V_i}{(\pi/2) I_o + \left((2P_o)/(V_1 I_o)\right)}
\]
By using (12), (7) and selecting \(f_{sw}\), \(C_o\) and \(L_r\) are calculated.

### 3.2 Output capacitor \((C_o)\)

In PFC converters, the output voltage ripple cannot be compensated by the converter because the converter input current shape is sinusoidal. Therefore the output voltage has its spectrum dominated by a DC component (average value), a high-frequency component (because of switching action of the converter) and a low-frequency component (twice line frequency, because of oscillating single-phase power at the input). Considering the worst case, the output capacitor must compensate the \(2f_m\) frequency ripple. As a result, \(C_o\) can be obtained from the following equation
\[
C_o = \frac{P_o}{f_m \cdot V_o \cdot \Delta V_o} = 1000 \mu F
\]
where \(f_m\) is the input frequency and \(\Delta V_o\) is the output ripple. Maximum ratings of semiconductor elements.

The maximum switch voltage and current can be obtained from following equations
\[
V_{SW, max} = V_i + V_o
\]
\[
V_{O3, max} = 2(V_i + V_o)
\]
\[
I_{SW1,2, max} = I_i + I_o + \frac{\Delta I_1}{2} + \frac{\Delta I_3}{2}
\]
\[
I_{D3, max} = I_o + \frac{\Delta I_3}{2}
\]
where \(V_1\) and \(I_i\) are the input voltage and current peaks, respectively.

### 3.3 Control circuit

In general the control method of this converter can be the same as a conventional PWM-PFC. For simplicity, peak current mode control is used in this paper as shown by the block diagram of controller in Fig. 6. Thus conventional PFC control ICs can be employed. The only difference between conventional PFC controller ICs and the controller of the proposed converter is the existence of a monostable to produce auxiliary switch gate signal. Based on the converter operation explained in the previous section, the on time of monostable must be selected equal to \(0.75T_r\) (where \(T_r\) is \(1/f_i\)). It must be noted that similar to the conventional PFC, the voltage loop cannot compensate the \(2f_m\) output voltage ripple. Thus the voltage loop must be designed, so that the control circuit would neglect the \(2f_m\) ripple.

### 4 Simulation results

The proposed bridgeless SEPIC PFC is simulated by PSIM when \(V_{AC} = 220\ V_{rms}\), \(V_o = 150 \pm 5\ V_{DC}\), \(f_{sw} = 100\ kHz\) and 450 W output power. According to the above design considerations, the main circuit element values are \(C_1 = C_2 = 1\ \mu F\), \(L_1 = L_2 = 2\ mH\), \(L_3 = 1\ mH\), \(C_o = 1000\ \mu F\). The resonant elements, \(C_r\) is equal to 5 \(nF\) and \(L_r\) is equal to 10 \(\mu H\). It must be noted that in selecting resonant elements, (7) is not considered in order to make the switching transient times observable in the waveforms. Thus, the resonant frequency is selected five times greater than the switching frequency.

Fig. 7a shows the input current and voltage at full load simultaneously. It can be observed from this figure that input current is in phase with the input voltage and is practically sinusoidal with low total harmonic distortion (THD) and high-power factor. Also Fig. 7b shows the input current in frequency domain. It can be observed from this figure that the input current harmonics are below IEC61000-3-2 standard. Fig. 8a shows that the main switch turn on and off are under ZVS condition. \(D_3\) turns on under zero-current and zero-voltage conditions and turns off under zero voltage condition as it is shown in Fig. 8b.
the reverse recovery and switching losses of the main diodes are reduced by employing the proposed converter. The switching waveforms of the auxiliary switch $S_3$ is shown in Fig. 9.

5 Experimental verification

A prototype of the proposed converter with the specifications used in the simulation of PFC converter (in the previous section) is implemented to show the validity of theoretical analysis and simulation results. The proposed bridgeless SEPIC PFC converter is realised by IRFP460 for switches and MUR1660 for all diodes except MUR8100 for $D_3$.

The experimental results of input line current and input line voltage are shown in Fig. 10 for 110 and 220 $V_{\text{rms}}$ input line voltage. The waveforms of input voltage and current are almost in phase and the measured power factor is near unity especially when the input voltage is fully sinusoidal. Also the measured THD of the input current is near zero. The commutation waveforms of $S_1$ and $D_3$ are shown in Fig. 11. This figure shows that $S_1$ and $D_3$ are turned on and off under ZVS condition because of added auxiliary circuit. There are some ringing at turn off instant of $D_3$. It is because of resonant between resonant element and junction capacitance of $D_3$. However, it must be noted that, because of zero voltage turning off, the switching losses are reduced. The zero level of each channel is shown by '1',

Fig. 7  Graphs showing
a Top: line voltage, bottom: input line current
b Input current harmonics

Fig. 8  Voltage and current waveforms of
a Switch $S_1$
b Diode $D_3$ in a switching cycle

Fig. 9  Voltage and current waveforms of $S_3$
‘2’ and ‘3’ on the left side of each figure. The switching waveforms of auxiliary switch $S_3$ are shown in Fig. 12. $S_3$ is turned on under ZCS condition and is turned off under ZVS and ZCS condition. Fig. 13 shows the output peak to peak voltage ripple is below 5 V at 150 VDC and 450 W output power which confirms the design goals. In comparison to simulation results, there is some ringing and spikes in experimental results. This is because of the resonance between the junction capacitances of semiconductor elements and parasitic inductances.

Based on simulation results, the efficiency of the proposed PFC converter is improved by about 3% in comparison with the conventional SEPIC PFC converter at full load. Efficiency comparison between the proposed bridgeless SEPIC PFC and the conventional SEPIC PFC is provided in Fig. 14.

6 Conclusions

A new ZVT SEPIC PFC converter is introduced in this paper. This converter has reduced conduction and switching losses
because of employing bridgeless and ZVT soft switching techniques simultaneously. The input current is sinusoidal and in phase with the input voltage. This converter is fully analysed and the computer simulations are presented. The simulation results show the validity of theoretical analysis. Measured power factor is near unity and THD near zero which satisfies the IEC61000-3-2 standard. A 450 W prototype of the proposed PFC rectifier is implemented to show the validity of simulation and theoretical analysis. The experimental results show that ZVS soft switching conditions for the main switch and diode are achieved and zero-voltage/zero-current switching conditions are achieved for the auxiliary circuit. The efficiency comparison between the proposed converter and the hard switching counterpart shows 3% improvement at full load.

7 References