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A high CMRR low noise CMOS amplifier for electrocardiogram signal recording applications

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Abstract: *Electrocardiogram signal and other biomedical signals are low frequency and low amplitude signals. This article proposes a high CMRR low noise wide linear output range biopotential CMOS amplifier for electrocardiogram signal recording applications and physiological measurement frontend. The wide linear output range is achieved by effectively combining the first-stage open-loop and the second-stage closed-loop configuration, and using additional gain enhancement switches. Due to the wide linear output range, the proposed amplifier shows a stable voltage gain of 46.3 dB for output range from 0.15 to 3.12 V and THD of 0.04% with a 15 mVpp input amplitude (all with 3.3 V supply).*

Keywords:CMOS amplifier, physiological measurement, rail to rail, biopotential amplifier.

1. Introduction

The electrocardiogram (ECG) is an important diagnostic tool in the detection and treatment of heart disease. Very large scale integration (VLSI) has made possible the aim of complete miniaturization of biomedical systems come true in today's era. ECG signal acquisition systems mainly require precision and quick acquisition of data. On chip systems enable portability, allowing the patient to be freed from long wires. ECG signals and other biomedical signals are low frequency and low amplitude signals. Transmission and acquisition of these signals when miniaturization is also targeted, pose major challenges with respect to low power consumption, high CMRR, low cost, low input referred noise, etc. The front end of the acquisition system is an instrumentation amplifier suitable for biomedical signal acquisition.
An ECG signal can vary in magnitude from patient to patient and can typically be in the range of 80-2000µV [3],[14],[15],[16].This will require the signal to be amplified several hundred times before it is sampled. In this case to achieve an output voltage range of 0-4 volts a gain of 750 is required. The small voltage of the ECG also makes it vulnerable to many types of noise.The requirements for a 6-Lead ECG acqui- sition device, therefore uses 3 electrodes to collect voltages from the body, since each lead is a differential measurement between the electrodes. Using Eindhoven's triangle for electrode placement and lead derivation, the three leads Lead I, Lead II and Lead III can be obtained [3]. However it is not necessary to amplify all three signals as Lead I1 can be derived from the addition of Lead I and Lead III. The augmented leads aVR, aVL, aVF can also be found through similar calculation. Therefore the hardware is only required to produce ECG Signals for Lead I and Lead III. Since the voltages and currents from the electrodes are small in magnitude the amplifier input impedance must be very high. This requires the use of instrumentation amplifiers, due to their low impedance, good CMRR and low noise features.

The key element of the measurement frontend is the biopotential amplifier that determines the overall performance of the measurement system. To amplify weak and noisy biopotentials without loss, amplifiers require stable gain, low noise, high common mode rejection ratio (CMRR), and high input impedance. In addition, the amplifier requires a wide linear output range to maintain a high dynamic range for the measurement frontend by maximizing the input range of the ADC. The linear output range of an amplifier is defined as the output range with constant voltage gain, in other words the output range without distortion. Fig. 2 shows the

amplifier transfer characteristic with a wide and a narrow linear output range. A wide linear output range is preferred, since poor amplifier output range can lead to higher ADC resolution and higher power consumption to maintain the required signal-to-noise ratio of the measurement frontend [4], [5]. The linear output range of the amplifier is critically limited by voltage gain reduction with output level variation. The gain reduction is mainly caused by output resistance variation of the output-stage transistors as the drain to source voltage change. This is much severe for cascode output stages, which will significantly reduce the linear output range of the amplifier [6]–[8]. Moreover, this will be one of the major non idealities that will critically degrade the performance of the biopotential amplifiers as the transistor sizes continue to scale down and the supply voltage further reduces. However, not much research has been focused on improving the linear output range of biopotential amplifiers, yet a lot of research has been emphasized on reducing the input offset and noise, and improving the CMRR. So far, among the amplifiers, the current-mode instrumentation amplifier (CMIA) is the most widely used architecture for biopotential measurements due to low power, low noise, and high CMRR [9], [10]. Although CMIAs are widely used for biopotential amplification, to obtain a wide linear output range, an additional rail-to-rail output stage or a fully differential design is required, which can increase the power and the silicon area [11], [12]. The differential difference amplifier (DDA)-based instrumentation amplifiers (IAs) can achieve high CMRR; however, DDAs require extra circuit components, such as the class AB output stage to drive the feedback resistors and the common-mode (CM) feedback loops, which eventually leads to higher power and larger silicon area [13]–[15].

2. Amplifier architectture

The proposed amplifier architecture consists of the first-stage open-loop and the second-stage closed-loop configuration that is shown in fig.1. The circuit block within the dotted line shows the external high-pass filter that is used to eliminate the dc offset originating from the skin-electrode interface. The first stage consists of the rail-to-rail differential amplifier and two voltage buffers. The second stage includes the closed-loop class-A amplifier (M_{11} and M_{12}), a voltage buffer and two gain enhancement switches (M_9 and M_{10}). As shown, the first stage is efficiently combined with the second-stage closed-loop amplifier. The first-stage nMOS input pair drives the second-stage pMOS amplifier, and vice versa, where the drain of M_{11} and M_{12} is tied together for the output generation. This eliminates using two separate second-stage amplifiers for each first-stage nMOS and pMOS input pairs, which leads to a compact amplifier architecture. The first-stage open-loop maintains a high input impedance, whereas the second-stage closed-loop minimizes the overall amplifier gain reduction with output level variation. However, due to the closed-loop configuration, the second-stage input resistance is not high.Hence, this will decrease the first-stage gain.

To prevent this problem, voltage buffers are added to the first-stage output node. Another buffer placed at the second-stage output node alleviates the loading effect that enables using small-sized feedback resistors. The operation of the proposed amplifier is divided into three regions depending on the input voltage levels V_{in+} and V_{in-} .In case the input voltage difference is small, $V_{in+} \approx V_{in-}$, the first-stage outputs V_1 and V_3 will be in the midsupply range, which is the CM level. As a result, the second stage will not experience much gain reduction, and both gain control switches M_9 and M_{10} will be inactive. In this case, the small signal output voltage of the nMOS input pair V_1 and the pMOS input pair V_3 can be expressed

$$v_1 = -A_{1n}.(v_{in+} - v_{in-}) \quad (1)$$

$$v_3 = -A_{1p}.(v_{in+} - v_{in-}) \quad (2)$$

Where A_{1n} and A_{1p} are the first-stage open-loop gain of nMOS and pMOS input pairs, respectively. Assuming the node voltages V_2 and V_4 are fixed to the CM voltage by the second stage feedback operation, the node equation at node V_2 and V_4 can be written as

$$\frac{v_1 - v_2}{R_1} = \frac{v_2 - v_{out}}{R_2} \quad (3)$$

$$\frac{v_3 - v_4}{R_3} = \frac{v_4 - v_{out}}{R_4} \quad (4)$$

Where unity buffer gains are assumed. The overall voltage gain is obtained by combining (3) and (4) with the equation relating *v*out with v_2 and v_4, which is given a

$$v_{out} = -gm_{11}(ro_{11} \| ro_{12})v_2 - gm_{12}(ro_{11} \| ro_{12})v_4 \quad (5)$$

Where gm_{11} and gm_{12} are the transconductance of M_{11} and M_{12}, and $ro11$ and ro_{12} are the output resistance of M_{11} and M_{12}, respectively. In addition, considering a symmetrical design, $gm_{11} = gm_{12}$, the second-stage open-loop gain is defined as

$$A_2 = -\frac{v_{out}}{v_2} = -\frac{v_{out}}{v_4} = gm_{11,12}(ro_{11} \| ro_{12}) \quad (6)$$

Where the node voltages V_2 and V_4 are assumed to be identical due to the second-stage feedback operation.

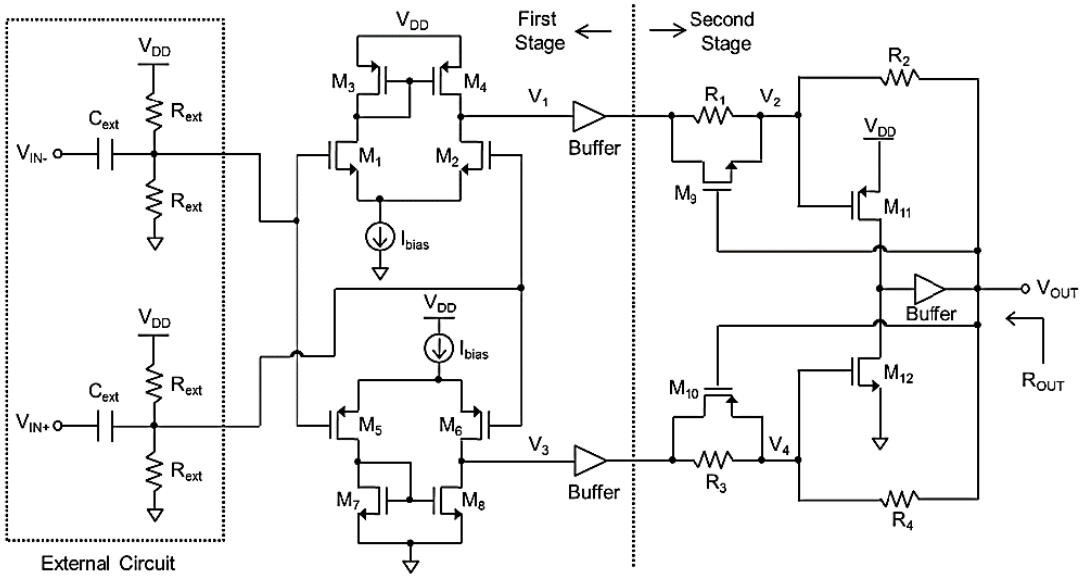

Fig. 1. Proposed amplifier architecture.

As a result, assuming the output resistance of the buffer R_{buff} is much less than R_1 and R_3, the overall voltage gain $v_{out} / (v_{in+} - v_{in-})$ is given as

$$A_{ov} = -\frac{(\frac{A_{1n}}{R_1} + \frac{A_{1p}}{R_3})}{\frac{1}{(R_2 \| R_4)} + \frac{1}{A_2}.[\frac{1}{(R_1 \| R_2)} + \frac{1}{(R_3 \| R_4)}]} \quad (7)$$

Furthermore, assuming $A_1 = A_{1n} = A_{1p}$, and $R_{1,3} << R_{2,4}$, the overall gain can be simplified as

$$A_{ov} = A_1 \cdot A_{2,cl} \quad (8)$$

Where $A_{2,cl}$ is the closed-loop gain of the second stage, $A2,cl = v_{out}/v_1 = v_{out}/v_3$ that is expressed as

$$A_{2,cl} \approx -\frac{(\frac{R_2 \| R_4}{R_1 \| R_3})}{1 + \frac{1}{A_2}.(\frac{R_2 \| R_4}{R_1 \| R_3})} \quad (9)$$

Therefore, if A_2 >>1, *A*ov will simply be the product of $A_1$and the resistor ratios $(R_2\|R_4) / (R_1\|R_3)$. In case the input voltage difference is large, V_{in+}>> V_{in-} or V_{in+} << V_{in-}, node voltages V_1 and V_3 will deviate from the midsupply level, and the amplifier output V_{out} will move toward the supply rails. This will either put M_{11} or M_{12} in the triode region by reducing the drain to source voltage, which will reduce *A*2. However, the gain enhancement switches M_9 and M_{10} will be activated depending on the amplifier output level V_{out}, which will modify the second-stage closed-loop gain as

$$A_{2,cl} \approx -\frac{(\frac{R_2 \| R_4}{R_1' \| R_3'})}{1 + \frac{1}{A_2}.(\frac{R_2 \| R_4}{R_1' \| R_3'})} \quad (10)$$

where $R_1' = (R_1 \| R_{ON,M9})$ and $R_3' = (R_3 \| R_{ON,M10})$ and when V_{out} is near GND, M_9 will be OF (RON,$M9$ =∞) and when V_{out} is near V_{DD}, M_{10} will be OFF (RON,M_{10} =∞). Therefore, R_1' and R_3'will compensate the overall gain degradation caused by A_2 reduction. For the proposed amplifier, to makeA_1 = 35 dB and A_2 = 30 dB, the tail bias current of the first-stage nMOS and pMOS input pairs is set to 0.7μA and the second-stage bias current is set to 1 μA. In addition, the size of the first-stage input devices M_1, M_2, M_5, and M_6, and the second-stage input devices M_{11} and M_{12} are set properly to obtain an identical *gm*. first-stage nMOS and pMOS input pairs is set to 0.7μA and the second-stage bias current is set to 1μA. In addition, the size of the first-stage input devices M_1, M_2, M_5, and M_6, and the second-stage input devices M_{11} and M_{12} are set properly to obtain an identical *gm*.
The value of *R*1, *R*3 and *R*2, *R*4 is set to 1 and 10 kΩ, respectively. This makes the resistor ratio $(R_2 \| R_4) / (R_1' \| R_3')$ equal to 10. Furthermore, the size of the gain enhancement switches *M*9 and *M*10 is set such that $R_1'$and R_3'vary symmetrically from 1 kΩ to 150 Ω as V_{out} varies within the output range of the amplifier. However, as *V*out moves toward the supply rails, node voltages V_2 and V_4 deviate from the midsupply level, 1.65 V. That is, for V_{in+} >> V_{in-}, V_{out} moves toward V_{DD} and node voltages V_2 and *V*4 approach 0 V, which turns ON M_9 and turns OFF M_{10}. On the other hand, for *V*in+ <<*V*in−, V_{out} moves toward GND, and node voltages V_2

and $V4$ approach V_{DD}, which turns OFF M_9 and turns ON M_{10}. This will cause an abrupt change in R_3' and R_3' as V_{out} approaches the supply rails due to the sudden increase in the gate to source voltage of M_9 and M_{10}. In fact, this is favorable for the overall gain linearity by providing a higher degree of compensation as $A2$ drastically reduces.

3. Results

Table.1 shows the measured performance of the proposed amplifier compared with state-of-the-art biopotential amplifiers, where for the biopotential recording ICs [24], [28], [29], only the frontend amplifiers are considered. The voltage gain of the proposed amplifier is the average value obtained from 10 different parts. CMRR is measured with and without the off-chip components (C_{ext}, R_{ext}), where CMRR drops to 76.5 dB with the off-chip components. However, this can be improved by using higher tolerance off-chip components (less than 1%). The tolerance of C_{ext} and R_{ext} used in the CMRR measurement is ±5%. In addition, the input referred noise is obtained within the amplifier bandwidth of 0.7 Hz–10 kHz. The proposed amplifier shows slightly better CMRR and comparable PSRR compare with other amplifiers, except for [26] that has the highest CMRR among the other amplifiers. In addition, the THD (0.04% for input amplitude of 15 mVpp) is better than other amplifiers, which is enabled by the wide linear output range. The input amplitude of 15 mVpp is sufficient to accommodate various extracellular biopotential signals. Although the input referred noise of the proposed amplifier is slightly higher than the state-of-the-art amplifiers, the noise efficiency factor (NEF) is comparable with [24] and [26], which is a result of the power efficient design. Obviously the 3.3 V supply leads to a higher power consumption, however, due to the rail-to-rail input stage, proper operation is observed with reduced supply voltage (~1.5 V). Furthermore, the proposed amplifier (even with the 0.35-μm technology) shows small area compared with [24], [26], and [29].The small area is obtained by the compact amplifier architecture and efficient design optimization. The input offset of the proposed amplifier varied from 0.18 to 2.47 mV with average of 1.31 mV for 10 different chips. Dummy devices and common centroid layout techniques are applied for the Nmos and pMOS input pairs, and relatively large size devices ($W{\cdot}L$) of 100 μm^2 (nMOS) and 300 μm^2 (pMOS) are used to improve the matching and eventually reduce the input offset. Overall, although the linear output range of the proposed amplifier can be effectively extended while achieving a reasonable CMRR and NEF, still several demerits of the design exist. First, the first-stage open-loop configuration can be more sensitive to mismatch for advanced CMOS technology. Second, the on-chip implementation of the external electrode offset cancellation circuitry can increase the core area, and finally, an additional amplifier input offset cancellation scheme can be required for extremely low amplitude biopotential acquisition.

Table.1.The measured performance of the proposed amplifier compared with other biopotential amplifiers.

Ref.	[24]	[25]	[26]	[27]	[28]	[29]	**This work**
Technology	CMOS 65nm	CMOS 0.13µm	CMOS 0.18µm	CMOS 0.13µm	CMOS 0.18µm	CMOS 0.18µm	**CMOS 0.35µm**
Gain (dB)	32	40	40 – 70	40	30 - 72	52	**46.3**
CMRR (dB)	75	80	120	78	60	73	**85.0**
PSRR (dB)	64	80	-	80	76	80	**83.2**
THD (%) @ Input amplitude	1% @ 0.2mV$_{rms}$	1% @ 1mV$_{pp}$	-	1% @ 16.5mV$_{pp}$	1% @ 18mV$_{pp}$	0.59% @ 2mV$_{pp}$	**0.04% @ 15mV$_{pp}$**
BW (kHz)	10	10.5	0.1	19.9	0.2	10	**10**
Input referred noise (µV$_{rms}$)	4.9	2.2	0.88	3.7	3.2	3.2	**5.16**
NEF	5.3	2.9	4.7	3.04	2.72	1.57	**4.79**
Supply voltage (V)	0.5	1.0	0.4	1.5	1.8	0.45	**3.3**
Current (µA)	8.26	12.1	0.22	2.6	10.7	1.62	**5.6**
Power (µW)	4.13	12.1	0.09	3.9	10.48	0.73	**18.5**
Area (mm^2)	0.0037	0.072	0.28	0.03125	-	0.1*	**0.063**

Along with the basic electrical characteristics, the proposed amplifier is simulated using ECG signals. The ECG signal used as the amplifier input are obtained from OP_AMP based ECG simulator was introduced by Bashir Najafabadian et al, that is presented in fig.2. For more details refer to [15]. However, to show the amplifier output waveform within the full output range, the amplitude of the ECG input was adjusted for the simulation. In addition, to make the simulation setup similar to the human subject, an equivalent impedance of Req = 500 kΩ and Ceq = 1µF obtained from the standard skin electrode interface is connected to the amplifier input node [23]. Fig. 3 shows the output waveform of the proposed amplifier with ECG simulator input. The output waveforms for input do not show distortion, and the Q, R, S, and T waves are clearly shown.

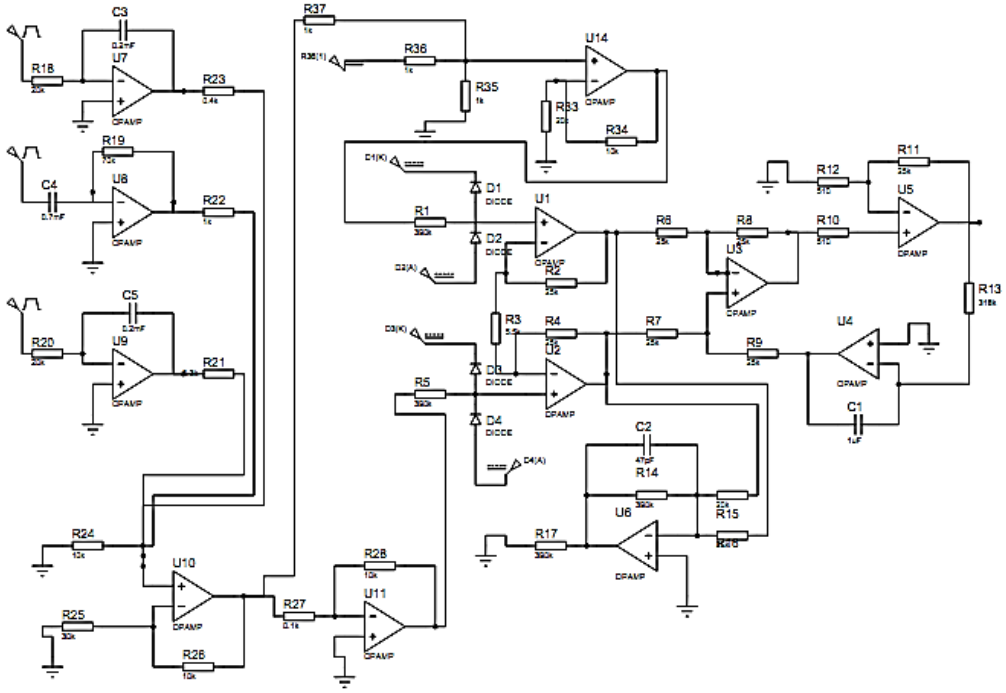

Fig.2 ECG simulator architecture.

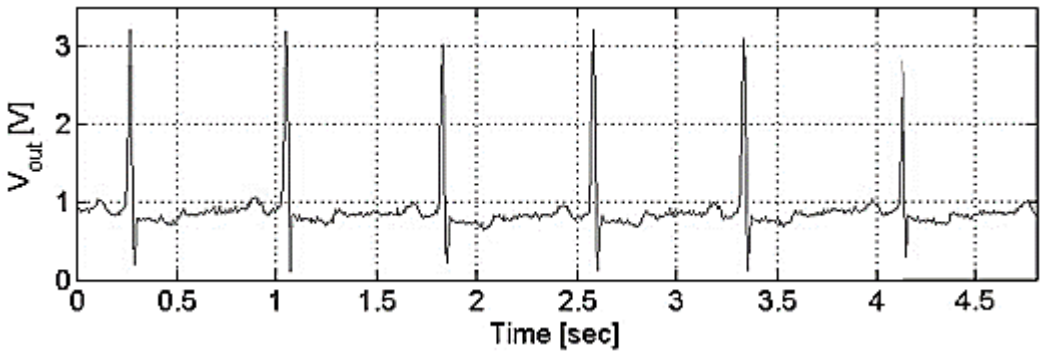

Fig. 3 Output waveform of the proposed amplifier with ECG simulator input.

3. Conclusion

In this paper, we propose a wide linear output range biopotential amplifier for physiological measurement frontend. The wide linear output range is achieved by effectively combining the first-stage open-loop and the second-stage closed-loop configuration, and using additional gain enhancement switches. Due to the wide linear output range, the proposed amplifier shows a stable voltage gain of 46.3 dB for output range from 0.15 to 3.12 V and THD of 0.04% with a 15 mVpp input amplitude (all with 3.3 V supply). In addition, the voltage gain and linear output range of the proposed amplifier do not significantly change with different process corners, and the CMRR and PSRR are not sensitive to feedback resistor mismatch. Furthermore, both the simulation and measurement results demonstrate the proper operation of amplifier with actual physiological signals. Overall, with a signal bandwidth of 10 kHz, the proposed amplifier is suitable for ECG, EEG, and electromyogram measurement frontends, where the dynamic range will be extended by maximizing the input range of the ADC. However, although the proposed amplifier is realized with a CMOS technology with supply voltage of 3.3 V, it can be simply adopted to advanced CMOS technologies with lower supply voltages.

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